Input Filter Damping: Sizing Rd and Cd to an Impedance Target

Philip Bassett · AN2026-03 · Revised 25 September 2026
https://switchmode.io/resources/input-filter-damping

An undamped input filter resonates, and a regulating converter looks like a negative resistance at its input. Put the two together and the bus oscillates. The fix is a damping resistor R_d in series with a blocking capacitor C_d, connected across the filter capacitor. This note starts from a filter that already exists. It finds the smallest R_d and C_d that hold the filter's output impedance under a stated limit, and the power rating the resistor needs.

Three things here aren't in the usual references. The published design procedures run forwards, from a damping capacitor you picked to the impedance you got. This note inverts them and picks the capacitor from the impedance you need. Three separate references say the blocking capacitor is there to avoid dissipation in the resistor, and none of them says how much is left. This note bounds it in one line. And the resistor turns out to be the loose tolerance and the capacitor the tight one. That's the opposite of how the usual rule of thumb is applied.

This note sizes the damping for a filter you already have. Choosing the filter itself is the other half, and Input Filter Design: The Inductor Sets Your Stability Margin does that.

Before you start: do you need a damping network?

A real filter is never undamped. The inductor's DC resistance and the capacitor's equivalent series resistance (ESR) already damp it, and sometimes they damp it enough. Check that first:

$$Q = \frac{R_0}{R_L + R_C} \qquad |Z_o|_{pk} \approx R_0 Q = \frac{R_0^2}{R_L + R_C}$$

where:

- Q is the quality factor of the filter with no damping network fitted.
- $|Z_o|_{pk}$ is the peak of the filter's output impedance Z_o. That's the impedance the converter sees looking back into the filter, with the source shorted.
- $R_0 = \sqrt{L_f / C_f}$ is the filter's characteristic impedance, from step 1.
- L_f is the filter inductance, and C_f is the filter capacitance at the bus voltage.
- R_L is the filter inductor's DC resistance.
- R_C is the filter capacitor's ESR.

That estimate is good to better than 2% for any Q above 5, and better than 0.5% above 10. If $R_0 Q$ is already under the limit from step 2, fit nothing.

It rarely is. In the worked example, a 25 mΩ inductor and a 3 mΩ ceramic leave Q = 73. That's a 149 Ω peak against a limit of 5.77 Ω.

Two other fixes come before a damping network, and both are free. **A more resistive inductor damps the filter at no component cost**, though it costs efficiency in the DC current. **A different split of the**

same $L_f C_f$ product changes R_0 directly, and the peak scales with it. If step 3 asks for a damping capacitor you can't fit, that split is what to change.

What you need

- L_f **and** C_f, with C_f taken at the bus voltage, not from the label. A class II ceramic loses a large part of its capacitance under DC bias. The example's 4.7 µF 100 V X7R is 2.4 µF at 48 V.
- **The inductor's DC resistance and the capacitor's ESR**, for the check above.
- **The converter's input power and its minimum bus voltage.** Both set the impedance you have to stay under.
- **The margin you're designing to**, in dB. 6 dB is the usual figure in aerospace and military work [7].
- **The AC ripple voltage across the filter capacitor**, measured or calculated. Step 5 needs it.
- **The ESR of the damping capacitor**, if you plan to use an electrolytic. It's part of R_d.

STEP 1

Characteristic impedance and corner frequency

$$R_0 = \sqrt{\frac{L_f}{C_f}} \qquad\qquad f_0 = \frac{1}{2\pi\sqrt{L_f C_f}}$$

where:

- R_0 is the filter's characteristic impedance.
- f_0 is its resonant frequency, which is also its corner frequency.
- L_f is the filter inductance.
- C_f is the filter capacitance at the bus voltage, not the value on the label.

Everything that follows is normalised to R_0.

STEP 2

The peak you're allowed

Inside its control bandwidth a converter holds its input power constant, so its incremental input resistance is negative:

$$R_N = -\frac{V_{in}^2}{P_{in}}$$

where R_N is the converter's incremental input resistance, V_{in} is its input voltage, and P_{in} is its input power. P_{in} is the output power divided by the efficiency.

Middlebrook's criterion says the filter's output impedance has to stay well below that magnitude at every frequency [6]. With a margin, the filter's peak output impedance must stay under

$$Z_{pk} = \frac{|R_N|}{10^{m/20}}$$

where Z_{pk} is the largest peak output impedance the filter is allowed, $|R_N|$ is the magnitude of R_N, and m is the margin in dB.

At 6 dB the divisor is 1.995, not 2. Evaluate $|R_N|$ at the **minimum** bus voltage, which is where it's smallest. If the bus has a wide range, run steps 1 to 4 at both ends. C_f falls as the bus rises, and that pushes R_0 the other way.

What "well below" should mean is a longer argument than this note. Middlebrook Stability Criterion: Why Failing It Doesn't Mean Your Converter Is Unstable works through seven criteria that answer it.

STEP 3

The damping capacitor

Define $n = C_d/C_f$, the ratio of the damping capacitance to the filter capacitance. With the damping resistor at its optimum for that n, the peak output impedance is [1], [2]:

$$\frac{|Z_o|_{pk}}{R_0} = \frac{\sqrt{2(2+n)}}{n}$$

where $|Z_o|_{pk}$ is the filter's peak output impedance, R_0 is its characteristic impedance from step 1, and n is the capacitance ratio.

Every published procedure uses that forwards. You choose n, usually 4 because that's the rule of thumb, and find out what peak you got. Run it the other way instead. Write $k = Z_{pk}/R_0$, which is the allowed peak from step 2 as a multiple of R_0. Set $|Z_o|_{pk}/R_0$ equal to k, square both sides, and it's a quadratic in n:

$$k^2 n^2 - 2n - 4 = 0$$

Take the positive root, because n can't be negative:

$$n = \frac{1 + \sqrt{1 + 4k^2}}{k^2} \qquad\qquad C_d = n\,C_f$$

where:

- n is the smallest capacitance ratio that reaches the allowed peak.
- k is that peak as a multiple of R_0.
- C_f is the filter capacitance at the bus voltage.
- C_d is the damping capacitance needed. It charges to the full bus voltage as well, so it's also a value at bias.

That's the smallest damping capacitor that can reach the target, and it's exact.

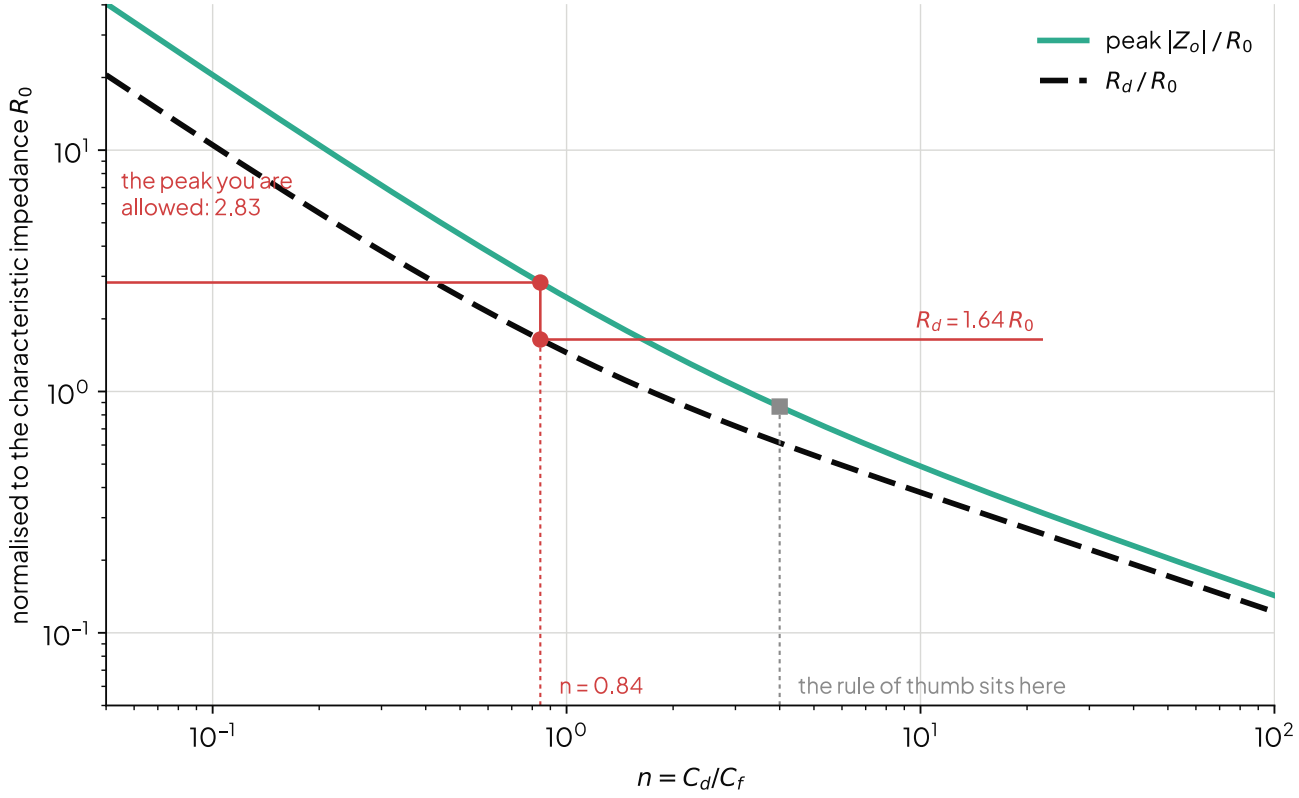

Fig. 1. Enter on the left at the peak you're allowed as a multiple of R_0, read down to n, read across to the resistor. The worked example needs 2.83 R_0, which is n = 0.84. The rule of thumb sits at n = 4, which buys 0.87 R_0 whether you needed it or not.

Two sanity checks on the result. For small k, meaning you're a long way above the target, $n \to 2/k^2$. **The damping capacitor grows as the square of how far you have to come down.** At k = 0.1 the exact answer is 202 and $2/k^2$ gives 200. For large k, $n \to 2/k$, and the capacitor becomes small.

If n comes out above about 10, stop. A damping capacitor ten times the filter capacitor means the filter is badly split, and resizing L_f and C_f is cheaper than buying the electrolytic. Part 2 covers that.

STEP 4

The damping resistor

For the n you just found, the resistance that minimises the peak is [1], [2], [3]:

$$R_d = R_0 \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}}$$

where R_d is the total series resistance of the damping branch, R_0 is the characteristic impedance from step 1, and n is from step 3.

Subtract the damping capacitor's ESR from that number, because the ESR is in series with the resistor and does the same job. With a ceramic C_d the ESR is a few milliohms and you can ignore it. With an aluminium electrolytic it can be most of R_d, or more than all of it. Then that capacitor can't reach the optimum, however small a resistor you fit next to it. The other way round, an electrolytic whose ESR lands near R_d needs no resistor at all.

The peak lands at

$$f_m = f_0\sqrt{\frac{2}{2+n}}$$

where f_m is the frequency of the peak output impedance, f_0 is the resonant frequency from step 1, and n is the capacitance ratio. f_m is below f_0, and it moves further below it as n grows. Measure there.

$R_d = R_0$ **is not the optimum.** It's the common rule of thumb, and it's only right near n = 1.73. At n = 4 the optimum is 0.61 R_0, and at n = 0.84 it's 1.64 R_0.

Nothing here costs you attenuation. At high frequency the branch looks like R_d in parallel with C_f. That's a lower impedance than C_f alone, so the filter attenuates marginally more than it did. In the worked example, 47.45 dB becomes 47.48 dB. The two alternatives use a damping inductor instead of C_d. A resistor and inductor in series, across the filter inductor, costs high-frequency attenuation by a factor of $1 + 1/n$. Here n is the damping inductance over L_f. The other puts a resistor in series with the filter inductor, with an inductor across it to carry the DC. It can't get the peak below $\sqrt{2}R_0$ with any inductor [1]. Those are the reasons to prefer this network.

STEP 5

What the resistor dissipates

Erickson [1], Sclocchi [3] and TI SNVA801 [4] all say the blocking capacitor is there to avoid dissipation in R_d. None of them says how much is left. It isn't zero. C_d blocks the DC, and the converter's ripple current goes straight through it.

The damping branch sees the ripple voltage across the filter capacitor. Each harmonic of that ripple drives a current of $V_h/\sqrt{R_d^2 + (1/\omega_h C_d)^2}$ through the branch, so

$$P_{Rd} = \sum_h \frac{V_h^2\, R_d}{R_d^2 + \left(\dfrac{1}{\omega_h C_d}\right)^2} \le \frac{V_{ac,rms}^2}{R_d}$$

where:

- P_{Rd} is the average power dissipated in the damping resistor.
- h is the harmonic number of the switching frequency: 1, 2, 3 and so on.
- V_h is the rms ripple voltage across C_f at harmonic h.
- $\omega_h = 2\pi h f_{sw}$ is the angular frequency of harmonic h, and f_{sw} is the switching frequency.
- R_d and C_d are the damping resistance and capacitance from steps 3 and 4.
- $V_{ac,rms} = \sqrt{\sum_h V_h^2}$ is the total rms ripple voltage across C_f, without its DC level, which C_d blocks.

The bound is one line, always true, and tight wherever the ripple sits well above the damping branch's own corner frequency, $1/(2\pi R_d C_d)$. That is normally all of it. In the worked example the bound is 0.2% above the harmonic sum. Use the bound.

You can put a scope on $V_{ac,rms}$. If the board doesn't exist yet, the fundamental carries most of it. For a buck:

$$I_{1,rms} = \frac{\sqrt{2}\, I_o}{\pi}\sin(\pi D) \qquad\qquad V_{ac,rms} \approx \frac{I_{1,rms}}{2\pi f_{sw} C_f}$$

where:

- $I_{1,rms}$ is the rms value of the fundamental of the converter's input current.
- I_o is the buck's output current.
- D is its duty cycle.
- f_{sw} is the switching frequency.
- C_f is the filter capacitance at the bus voltage.
- $V_{ac,rms}$ is the total rms ripple voltage across C_f.

The first form treats the input current as rectangular pulses of height I_o, which ignores the inductor's current ripple. The second takes all of that current into C_f.

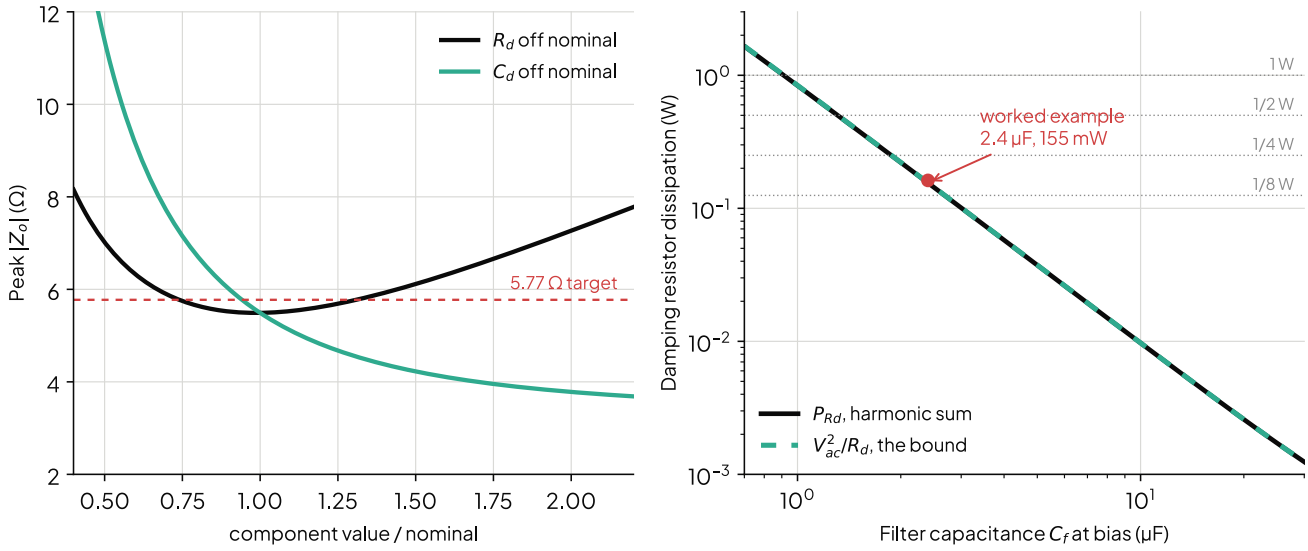

Fig. 2. Right: the same 200 W converter and the same 6 dB target, with the filter capacitance swept and the damping network resized each time. The harmonic sum and the bound lie on top of each other. Dissipation falls as roughly C_f^{-2}, so it's milliwatts on a large filter capacitor and approaching a watt on a small one. Left: how far each component can drift before the peak moves, which is the subject of step 6.

The dissipation depends almost entirely on the filter capacitor. That's worth knowing before you pick a package, because the answer ranges over three orders of magnitude across filters that all meet the same criterion.

STEP 6

Put the margin on the capacitor, not the resistor

The optimum in step 4 is flat and the constraint in step 3 is a cliff. Fig. 2 shows both. Halving R_d or doubling it costs about 2 dB. Losing 20% of C_d costs 1.3 dB, and losing 40% costs 4.0 dB.

That asymmetry decides where the tolerance goes. **Size n from the worst-case C_d**, meaning after tolerance, DC bias and end of life, and then let the resistor be a standard value. In the worked example, allowing both capacitors to run 20% low moves n from 0.84 to 0.96 and R_d from 3.35 Ω to 3.40 Ω. The capacitor has to grow by 14%. The resistor barely moves.

It also explains why n = 4 has survived as a rule of thumb. It's over-specified for most targets, and being over-specified is what makes it insensitive.

STEP 7

Check it

- **Sweep or simulate** $|Z_o|$ with the source shorted, and confirm the peak and its frequency. Include the DC resistance and the ESR. They only help.
- **Confirm the attenuation** at the switching frequency hasn't moved.
- **Measure the ripple across** C_f on the built board and redo step 5 with the real number.
- **Check the resistor's temperature** at full load, after the board has reached steady state.

WORKED EXAMPLE

A 200 W buck: 48 V bus, 12 V at 16 A, 500 kHz, 96% efficient. The filter is already on the board. The inductor is 10 µH with 25 mΩ of DC resistance. The capacitor is a 4.7 µF 100 V X7R with 3 mΩ of ESR, and its bias curve gives 2.4 µF at 48 V.

1. **Characteristic impedance.** $R_0 = \sqrt{10\,\mu\text{H}/2.4\,\mu\text{F}}$ = **2.04 Ω**, and f_0 = 32.5 kHz. The filter gives 47.5 dB at 500 kHz. Undamped, $R_0 Q$ = 149 Ω, so it needs damping.
2. **The peak allowed.** P_{in} = 200 W, so $|R_N| = 48^2/200$ = 11.52 Ω. At 6 dB, Z_{pk} = **5.77 Ω**.
3. **The capacitor.** k = 5.77/2.04 = 2.83, so $n = (1 + \sqrt{1 + 4(2.83)^2})/2.83^2$ = **0.84**, and C_d = 2.02 µF at bias.
4. **The resistor.** 1.64 × 2.04 Ω = **3.35 Ω**. The peak will sit at 27.3 kHz.
5. **Dissipation.** $I_{1,rms}$ = 5.09 A at 500 kHz, which puts 0.68 V rms across C_f. Summing the harmonics gives 0.72 V, so $P_{Rd} \le 0.72^2/3.35$ = **0.16 W**.
6. **Tolerance.** Allow 20% low on both capacitors and C_d has to be 2.31 µF nominal at bias.
7. **What to fit.** A second 4.7 µF 100 V X7R, identical to the filter capacitor, gives 2.4 µF at bias and n = 1.00 exactly. Its optimum resistor is 2.96 Ω, so fit **3.0 Ω**. That's 0.17 W, so a half-watt chip.

The result peaks at **4.78 Ω** at 26.7 kHz, which is 7.6 dB below the converter's input impedance against the 6 dB asked for.

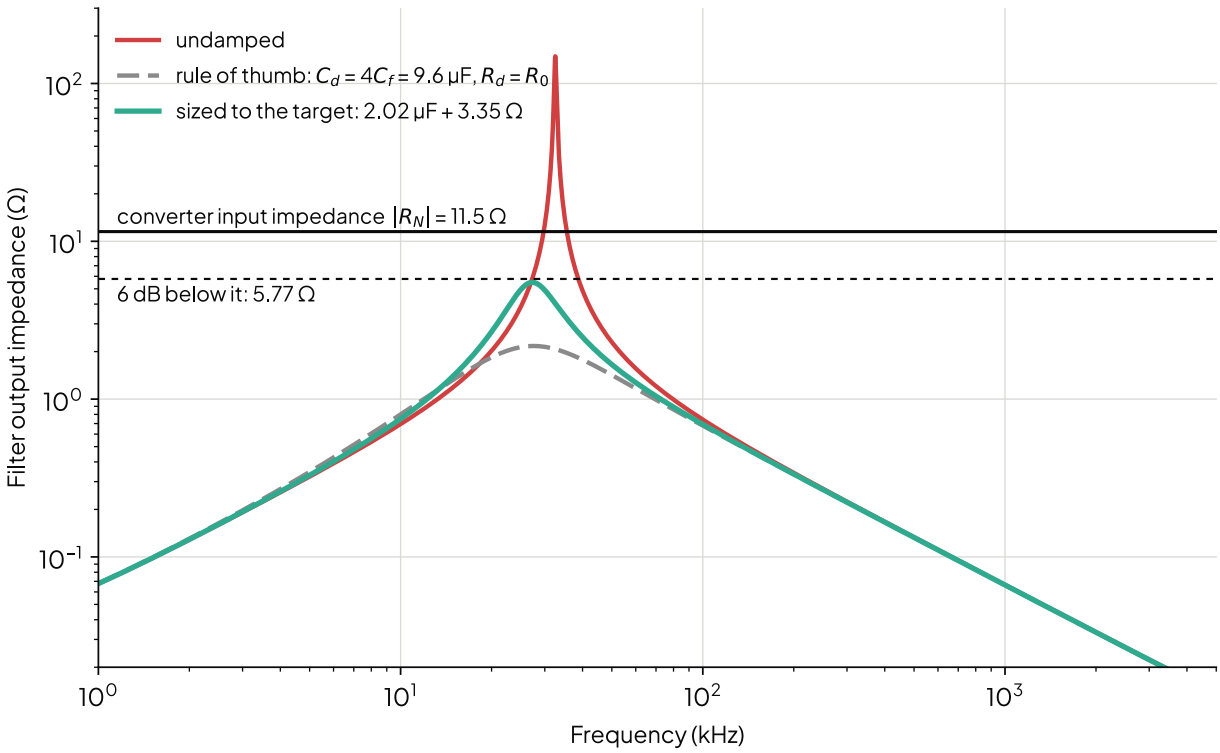

Fig. 3. Simulated with the DC resistance and ESR included. Undamped, the filter goes straight through the converter's 11.5 Ω. Sized to the target it touches 5.77 Ω. The rule of thumb, $C_d = 4C_f$ with $R_d = R_0$, reaches 2.17 Ω using 9.6 µF. That's 4.7 times the damping capacitance, for 8.5 dB of margin nobody asked for.

The rule of thumb isn't wrong here. It's expensive. It reaches 2.17 Ω when 5.77 Ω would have done. On a 48 V bus, that extra 7.6 µF is a part you have to find room and voltage rating for. It's also not at its own optimum: with the right resistor for $n = 4$, the same 9.6 µF would reach 1.72 Ω.

If you're working from Power Tip #4

Kollman's chart [5] is the only published way to run the design backwards, and it's the method this note replaces with an equation. Its worked example doesn't hold up, so check anything you read off it.

The example takes a 10 µH and 10 µF filter, so $R_0 = 1\,\Omega$, feeding a 12 W supply at 12 V. That allows a 6 Ω peak, and the chart is entered at $k = 6$. In this note's symbols, the article reads off $n = 0.1$, so 1 µF, and $R_d/R_0 = 3$, so 3 Ω. (Kollman writes them as C_D/C_O and R_D/Z_O.) **That network peaks at 39.4 Ω, 16 dB above the target.**

The two values are inconsistent with each other, which points at the reading rather than the chart. The resistor is right: the exact optimum for a 6 Ω peak is 3.24 Ω. The capacitor isn't, and $n = 0.1$ can't reach 6 Ω with any resistor at all, because its own best is 20.5 Ω. The correct answer is $n = 0.362$, so **3.62 µF and 3.24 Ω**, which the equation in step 3 returns directly.

Assumptions and limits

- **One filter section, and a stiff source.** The output impedance is taken with the source shorted. A second section in front changes it, and Erickson gives the conditions under which it doesn't [1]. Cascaded stages and distribution buses behave differently again, which Middlebrook's Criterion in Practice covers.

- **A constant-power load.** $R_N = -V_{in}^2/P_{in}$ holds inside the converter's control bandwidth. Above it the converter's input impedance rises towards its open-loop value, and the criterion gets easier. If the filter resonance sits near or above the crossover frequency, this note is conservative.
- **The magnitude-only criterion.** Keeping $|Z_o|$ a fixed number of dB below the converter's input impedance $|Z_{in}|$ is sufficient, not necessary. A design that fails it can still be stable, and part 1 shows by how much.
- **Ripple modelled as a rectangular pulse train.** Step 5 ignores the inductor's current ripple, which makes the harmonics slightly pessimistic. It also ignores any capacitance local to the converter, which takes ripple that would otherwise reach the filter node. Both errors are in the safe direction. Measure the ripple on the built board.
- **Steady state only.** The dissipation figure covers the switching ripple. A bus step or a large load step rings the filter, and R_d absorbs that energy too. On a repetitively pulsed load, check the resistor's pulse rating as well as its continuous rating.
- R_d **assumed resistive at** f_m**.** True for any sensible chip resistor at tens of kilohertz.

What this means for switchmode.io

An impedance margin is a number, and it should be an input to the design rather than something you discover afterwards. That's the whole argument for sizing the damping network from the margin instead of a rule of thumb. It's also the argument switchmode.io is being built around. The input filter calculator takes the rail, the switching frequency and an attenuation target. It sizes the filter and its damping network, and reports the Middlebrook and GMPM margins it achieved. It has a check mode for a filter you already have, which is the case this note is written for.

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